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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/713,754	11/13/2003	Bruce W. McGaughy	188122001900	1629

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EXAMINER	
PIERRE LOUIS, ANDRE	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 11/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/713,754	MCGAUGHY ET AL.	
	Examiner	Art Unit	
	Andre Pierre-Louis	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 08/28/2006 has been received and fully considered; claims 34-35 are added and now claims 1-35 are presented for examination.

Response to Arguments

2. Applicant's arguments filed 08/28/2006 have been fully considered but they are not persuasive.

2.1 Applicant argues that the combined reference cited do not teach the port connectivity interface, as claimed, and do not teach a set of load vector and the array, although it somewhat agrees that Zhou et al. connectivity refers to static database, the examiner asserts that Tcherniaev et al. teaches the sharing of dynamic information, such voltage between two or more subcircuits, which requires the port connectivity interface for that purpose (*see the cited figs., col., lines, along with col.col.14 lines 39-54 & col.16 line 35-col.17 line 47)* and further teaches a dynamic storage *(see fig.2). With* regards to the set of load vectors and the array of memory argued by the applicant, the examiner has specifically points out in the office below the portion of the prior art, which the examiner relies for teaching of these limitations, as both Tcherniaev et al. and Zhou et al. teach a matrix that includes a set of input, output vectors (*see fig.2B of Tcherniaev et al. and fig.3 of Zhou et al.*), and Tcherniaev et al. further teaches the set of load vectors (see *fig.11, 15(1526), col.9 lines 1-34 , col.19 line 39-50).*

2.2 While the applicant believes the independent claims along with their dependencies should be found allowable, the examiner respectfully disagrees and asserts that the combined teachings of the reference cited teach the entire claimed

invention. Found the applicant' s argument non-persuasive, the examiner maintains the rejection of the independent claims along with their dependencies.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

The claimed invention as a whole must accomplish a practical application. That is, it must produce a "useful, concrete and tangible result." State Street, 149 F.3d at 1373, 47USPQ2d at 1601-02. The purpose of this requirement is to limit patent protection to inventions that possess a certain level of "real world" value, as opposed to subject matter that represents nothing more than an idea or concept, or is simply a starting point for future investigation or research (Brenner v. Manson, 383 U.S. 519, 528-36, 148 USPQ 689, 693-96); In re Ziegler, 992, F.2d 1197, 1200-03, 26 USPQ2d 1600, 1603-06 (Fed. Cir. 1993)). Accordingly, a complete disclosure should contain some indication of the practical application for the claimed invention, i.e., why the applicant believes the claimed invention is useful. However, the mere fact that the claim may satisfy the utility requirement of 35 U.S.C. 101 does not mean that a useful result is achieved under the practical application requirement. The claimed invention as a whole must produce a "useful, concrete and tangible" result to have a practical application.

3.0 Claims 1-35 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The claims do not produce a useful, tangible, concrete result. ***See MPEP 2106 [R2]***

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4.0 Claims 1-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tcherniaev et al. (U.S. Patent No. 6.577.992), in view of Zhou et al. (U.S. Patent 6,807,520).

4.1 In considering the independent claims 1,12, and 23, Tcherniaev et al. substantially teaches a method of simulating a circuit, in particular the steps of: representing the circuit as a hierarchically arranged set of branches, including a root branch and a plurality of other branches logically organized in a graph *(see abstract, fig.2, col.8 line 1-62)*; the hierarchically arranged set of branches including a first branch that includes one or more driver leaf circuits and a second branch that includes one or more

receiver leaf circuits *(see abstract, fig.2, col.1 line 7-col.5 line 63 and col.8 lines 1-62);* wherein the first branch and second branch are interconnected in the graph through a third branch at a higher hierarchical level in the graph than the first and second branches *(fig.2, col.8 line 1-62, also col.1 line 7-col.5 line 63)*; and simulating operation of the one or more driver leaf circuits and the one or more receiver leaf circuits, together by using a port connectivity interface, without simulating operation of the third branch to determine a first set of changes in signal conditions shared by the one or more driver leaf circuits and the one or more receiver leaf circuits, wherein the port connectivity interface facilitates communication of dynamic information between the one or more driver leaf circuits and the one or more receiver leaf circuits, and wherein dynamic hierarchical data structures of the one or more driver leaf circuits and the one or more receiver leaf circuits are maintained *(fig.1-2, col.8 line 1-col.10 line 65).* Although Tcherniaev et al. does clearly state the term port connectivity interface, he teaches a rate of change of node voltage and the share of dynamic load which would require the port connectivity interface (*see the cited figs., col., lines, along with col.col.14 lines 39-54 & col.16 line 35-col.17 line 47*). Nevertheless, Zhou et al. substantially teaches a port connectivity where two subcircuits share one cut node Va (*fig.4, also see fig.9-10, col.12 line 58-col.14 line 60).* Tcherniaev et al. are analogous art because they are from the same field of endeavor and that the method and apparatus teach by Tcherniaev et al. is similar to that of the Zhou et al. Therefore, it would have been obvious to one ordinary skilled in the art at the time of the applicant's invention to combine the simulation method and system of Zhou et al. with the hierarchical data circuit simulation

of Tcherniaev et al. because Zhou et al. teaches the advantage of producing accuracy results *(col.2 lines 14-41), and* further teaches a simulation with simplified matrix computations and reduced amount of memory required to perform circuit simulation *(see col.2 lines 22-59).*

4.2 With regards to claims 2,13, and 24, the combined teachings of Tcherniaev et al. and Zhou et al. substantially teach that the simulating includes storing the first set of changes in signal conditions in a port connectivity interface and conveying the first set of changes in signal conditions from the one or more driver leaf circuits to the one or more receiver leaf circuits via the port connectivity interface *(see Zhou et al. fig.4, also see fig.9-10, col.12 line 58-col.14 line 60; also see Tcherniaev et al. col. col.16 line 35-col.17 line 47).*

4.3 Regarding claims 3,14, and 25, the combined teachings of Tcherniaev et al. and Zhou et al. teach that the port connectivity interface is generated dynamically upon detecting a set of triggering conditions during simulation *(see Tcherniaev et al. col.16 line 35-col.17 line 47 & col. 14 lines 39-54); also see examiner assumption noted in the rejection of claims 1,12,23, above, with regards to the port connectivity interface).*

4.4 As per claims 4,15, and 26, the combined teachings of Tcherniaev et al. and Zhou et al. teach that the port connectivity interface comprises: a set of input vectors for referencing to a set of input ports of the one or more receiver leaf circuits *(see Tcherniaev et al. fig.2B, col.9 lines 1-34; also see Zhou et al. fig.3);* a set of output vectors for referencing to a set of output ports of the one or more driver leaf circuits *(see Tcherniaev et al. fig.2B, col.9 lines 1-34; also see Zhou et al. fig.3)*; a set of load vectors

for referencing to a set of loads of the one or more driver leaf circuits *(see Tcherniaev et al. fig.2B, 11, col.9 lines 1-34 & also fig.15 (1526), col.19 line 39-50); also see Zhou et al. fig.3)*; and an array of storage elements for storing information associating the set of loads to the set of input ports *(see Tcherniaev et al. fig.2, 11, col.19 line 39-col.20 line 67)*.

4.5 Regarding claims 5,16, and 27, the combined teachings of Tcherniaev et al. and Zhou et al. teach that conveying the first set of changes in signal conditions comprises: monitoring the first set of changes in signal conditions at each output port of the one or more driver leaf circuits *(see Zhou et al. fig.1-2, 4-5, 8-10, col.1 line 24-col.3 line 21; also col.13 line 7-col.17 line 50), also see Tcherniaev et al. fig.2, 11-12, col.8 line 41-col.9 line 63)*; and communicating the first set of signal changes from the output ports of the one or more driver leaf circuits to the input ports of the one or more receiver leaf circuits through the port connectivity interface in response to the first set of changes in signal conditions exceed a first set of predefined tolerance *(see Zhou et al. fig.1-2, 4-5, 8-10, col.1 line 24-col.3 line 21; also col.13 line 7-col.17 line 50), also see Tcherniaev et al. fig.2, 11-12, col.8 line 41-col.9 line 63).*

4.6 As per claims 6,17, and 28, the combined teachings of Tcherniaev et al. and Zhou et al. teach that the first set of changes of signal conditions at each output port of the one or more driver leaf circuits comprises: a voltage of the output port *(see Zhou et al. fig.1-5, col.1 line 24-col.3 line 21, also col.13 line 7-col.17 line 50), also see Tcherniaev et al. fig.2, 11-12, col.8 line 41-col.9 line 63)*; a rate of change of voltage of the output port *(see Zhou et al. fig.1-5, col.1 line 24-col.3 line 21, also col.13 line 7-*

col.17 line 50), also see Tcherniaev et al. fig.2, 11-12, col.8 line 41-col.9 line 63); and a time stamp at which the changes of signal conditions occur *(see Zhou et al. fig.1-5, col.1 line 24-col.3 line 21, also col.13 line 7-col.17 line 50), also see Tcherniaev et al. fig.2, 11-12, col.8 line 41-col.9 line 63).*

4.7 With regards to claims 7,18, and 29, the combined teachings of Tcherniaev et al. and Zhou et al. teach that the step of communicating comprises: identifying input port references coupled to each output port of the one or more driver leaf circuits in accordance with the port connectivity interface *(see Zhou et al. fig.1-5, 8-10,* col.1 *line 24-col.3 line 21, also col.13 line 7-col.17 line 50), also see Tcherniaev et al. fig.2, 11-12, col.8 line 41-col.9 line 63);* identifying each input port of the one or more receiver leaf circuits that correspond to the input port references and transmitting the first set of changes in signal conditions from the one or more driver leaf circuits to the one or more receiver leaf circuits *(see Zhou et al. fig.1-5, 8-10, col.1 line 24-col.3 line 21, also col.13 line 7-col.17 line 50), also see Tcherniaev et al. fig.2, 11-12, col.8 line 41-col.9 line 63).*

4.8 Regarding claims 8,19, and 30, the combined teachings of Tcherniaev et al. and Zhou et al. teach the step of storing a second set of changes in signal conditions in the port connectivity interface and conveying the second set of changes in signal conditions from the one or more receiver leaf circuits to the one or more driver leaf circuits via the port connectivity interface (*see Zhou et al. fig.1-5, 8-10,* col.1 *line 24-col.3 line 21, also col.13 line 7-col.17 line 50), also see Tcherniaev et al. fig.2, 11-12, col.8 line 41-col.9 line 63).*

4.9 As per clams 9,20, and 31, the combined teachings of Tcherniaev et al. and Zhou et al. teach that conveying the second set of changes in signal conditions comprises: monitoring the second set of signal changes at each input port of the one or more receiver leaf circuits *(see Zhou et al. fig.1-2, 4-5, 8-10, col.1 line 24-col.3 line 21; also col.13 line 7-col.17 line 50), also see Tcherniaev et al. fig.2, 11-12, col.8 line 41-col.9 line 63)*; and communicating the second set of signal changes from input ports of the one or more receiver leaf circuits to output ports of the one or more driver leaf circuits via the port connectivity interface in response to the second set of change in signal conditions exceed a second set of predefined parameters *(see Zhou et al. fig.1-2, 4-5, 8-10, col.1 line 24-col.3 line 21; also col.13 line 7-col.17 line 50), also see Tcherniaev et al. fig.8-10, col.8 line 41-col.9 line 63).*

4.10 With regards to claims 10,21, and 32, the combined teachings of Tcherniaev et al. and Zhou et al. teach that the second set of signal changes at each input port of the receiver leaf circuit comprises: a current of the input port *(see Zhou et al. fig.1-5, col.1 line 24-col.3 line 21, also col.13 line 7-col.17 line 50), also see Tcherniaev et al. fig.8-10)*; a capacitance of the input port *(see Zhou et al. fig.1-5, col.1 line 24-col.3 line 21, also col.13 line 7-col.17 line 50), also see Tcherniaev et al. col.8 line 41-col.9 line 63)*; and a time stamp at which the second set of changes of signal conditions occur *(see Zhou et al. fig.1-5, col.1 line 24-col.3 line 21, also col.13 line 7-col.17 line 50), also see Tcherniaev et al. fig.2, 11-12, col.8 line 41-col.9 line 63).*

4.11 Regarding claims 11,22, and 33, the combined teachings of Tcherniaev et al. and Zhou et al. teach that that the step of communicating comprises: identifying load

references coupled to each input port of the one or more receiver leaf circuits in accordance with the port connectivity interface *(see Zhou et al. fig.1-5, 8-10,* col.1 *line 24-col.3 line 21, also col.13 line 7-col.17 line 50), also see Tcherniaev et al. fig.2, 11-12, col.8 line 41-col.9 line 63)*; identifying each output port of the one or more driver leaf circuits corresponding to the identified load references *(see Zhou et al. fig.1-5, 8-10, col.1 line 24-col.3 line 21, also col.13 line 7-col.17 line 50), also see Tcherniaev et al. fig.2, 11-12, col.8 line 41-col.9 line 63);* and transmitting the second set of signal changes from the one or more receiver leaf circuits to the one or more driver leaf circuit via the port connectivity interface *(see Zhou et al. fig.1-5, 8-10, col.1 line 24-col.3 line 21, also col.13 line 7-col.17 line 50), also see Tcherniaev et al. fig.2, 11-12, col.8 line 41-col.9 line 63).*

5. Claims 34-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tcherniaev et al., in view Zhou et al., as applied to claims 1-33 above, and further in view of Johannsen (U.S. Patent No. 5,910,898).

5.1 Regarding claims 34, Tcherniaev et al., as modified by Zhou et al. and applied to claims 1-33 teaches most of the instant invention; however he does not clearly teaches wherein communications of the dynamic information between the one or more driver leaf circuits and the one or more receiver leaf circuits comprise: a forward communication of changes in signal conditions from the one or more driver leaf circuits to the one or more receiver leaf circuits using the port connectivity interface without traversing the dynamic hierarchical data structure of the one or more driver leaf circuits and the one or more receiver leaf circuits. Johannsen substantially teaches a forward

and reverse communication of signals (*see fig.8-10, col.15 line 15-col.18 line 67*). Tcherniaev et al., Zhou et al. and Johannsen are analogous art because they are from the same field of endeavor and that the circuit design methods and tools teaches by Johannsen is similar to that of the method and apparatus of Tcherniaev et al. and the simulation system and method of Zhou et al. Therefore, it would have been obvious to one ordinary skilled in the art at the time of the applicant's invention to combine the circuit simulation methods of Johannsen with the method and apparatus of Tcherniaev et al. and the simulation system and method of simulation method of Zhou et al. because Zhou et al. teaches the advantage of producing accuracy results *(col.2 lines 14-41), and* further teaches a simulation with simplified matrix computations and reduced amount of memory required to perform circuit simulation *(see col.2 lines 22-59); and Johannsen* teaches the advantage to prove an improved circuit simulation tool that allow user to quickly design and automatically optimize large or complex design (col.1 lines 50-53).

5.2 As per claim 35, the combined teachings of Tcherniaev et al., Zhou et al., and Johannsen substantially teach the a reverse communication of changes in signal conditions from the one or more driver leaf circuits to the one or more receiver leaf circuits using the port connectivity interface without traversing the dynamic hierarchical data structure of the one or more driver leaf circuits and the one or more receiver leaf circuits (*see fig.8-10, col.15 line 15-col.18 line 67*).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

6.1 Morgan (U.S. Patent No. 6,083,271) teaches a method and apparatus for specifying multiple power domains in electronic circuit designs.

6.2 Bonitz (U.S. Patent No. 6,237,126) teaches an electrical analysis of integrated circuits.

7. Claims 1-35 are rejected and Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andre Pierre-Louis whose telephone number is 571-272-8636. The examiner can normally be reached on Mon-Fri, 8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul L. Rodriguez can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

November 1, 2006

APL

11/9/06

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